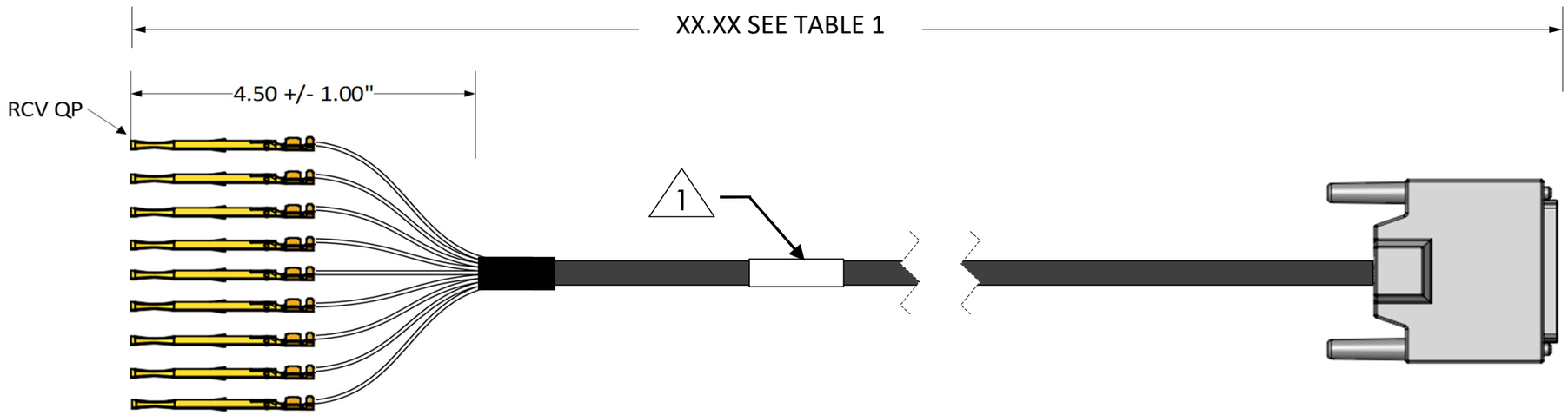
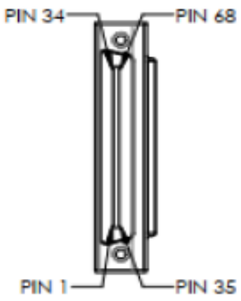
REV	DESCRIPTION	DATE	ENGINEER
A	ORIGINAL RELEASE #12606	5/17/2022	L SALE





68PN ML VHDCI OFFSET MATING FACE

TABLE 1	
PART NUMBER	LENGTH
VFLXXXXXX-020	20"
VFLXXXXXX-036	36"
VFLXXXXXX-048	48"
VFLXXXXXX-060	60"
VFLXXXXXX-072	72"

1. MARK IN APPROXIMATE AREA AS SHOWN "VFL138124-XXX REV [ ]"

NOTES:

DIMENSION DESIGNATOR LABELS PER ES6 UNLESS OTHERWISE SPECIFIED.

VPC BREAKOUT TOLERANCES UNLESS SPECIFIED REFERENCE ENGINEERING SPECIFICATION 4

IF	THEN
BUNDLE SIZE IS SMALLER THAN THE CONNECTOR ENVELOPE & STRAIN RELIEF IS OFFSET	3.50 +/ 1.00
BUNDLE SIZE IS SMALLER THAN THE CONNECTOR ENVELOPE & STRAIN RELIEF IS CENTERED	4.50 +/- 1.00
BUNDLE SIZE IS LARGER THAN THE CONNECTOR ENVELOPE	5.50 +/- 1.00

TORQUE ALL SCREWS PER ES2 UNLESS OTHERWISE SPECIFIED.

DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED.

RELAIMED CONNECTOR POSITIONS AND WIRE ROUTING ARE GENERIC AND MAY VARY WITH PINOUT

TOLERANCES UNLESS SPECIFIED

NOMINAL LENGTH	TOLERANCE
0 - 11.99"	+1.00/-0.00
12.00 - 59.99"	+2.00/-1.00
60.00 - 119.99"	+4.00/-1.00
120.00 - 299.99"	+6.00/-1.00
300.00" - UP	+5 %/-1.00

Virginia Panel Corporation

VFLSIG 68PN VHDCI ML TO QP

DWG.NO. VFL138124 REV A

SIZE	SCALE	CAGE CODE	SHEET
B	NONE	18117	1 OF 1

Run #	From Location (Pin)	From Signal Desc	Wire AWG	Wire Color	Wire Group (PAIR)	To Location (Conn-Pin)
1	68	FPGA 1, Connector 0, AI0+	30 T/P	WHT/RED	1	610138216
2	34	FPGA 1, Connector 0, AI0-	↑	RED/WHT	1	610138216
3	67	FPGA 1, Connector 0, AIGND0	26	SHIELD	1	610138216
4	67	FPGA 1, Connector 0, AIGND0	26	AI GND	-	610138216
5	66	FPGA 1, Connector 0, AI1+	30 T/P	WHT/BRN	2	610138216
6	32	FPGA 1, Connector 0, AI1-	↑	BRN/WHT	2	610138216
7	33	FPGA 1, Connector 0, AIGND1	30	SHIELD	2	610138216
8	65	FPGA 1, Connector 0, AI2+	30 T/P	WHT/PNK	3	610138216
9	31	FPGA 1, Connector 0, AI2-	↑	PNK/WHT	3	610138216
10	64	FPGA 1, Connector 0, AIGND2	26	SHIELD	3	610138216
11	63	FPGA 1, Connector 0, AI3+	30 T/P	WHT/ORG	4	610138216
12	29	FPGA 1, Connector 0, AI3-	↑	ORG/WHT	4	610138216
13	30	FPGA 1, Connector 0, AIGND3	30	SHIELD	4	610138216
14	62	FPGA 1, Connector 0, AI4+	30 T/P	WHT/YEL	5	610138216
15	28	FPGA 1, Connector 0, AI4-	↑	YEL/WHT	5	610138216
16	61	FPGA 1, Connector 0, AIGND4	30	SHIELD	5	610138216
17	60	FPGA 1, Connector 0, AI5+	30 T/P	WHT/GRN	6	610138216
18	26	FPGA 1, Connector 0, AI5-	↑	GRN/WHT	6	610138216
19	27	FPGA 1, Connector 0, AIGND5	30	SHIELD	6	610138216
20	59	FPGA 1, Connector 0, AI6+	30 T/P	WHT/BLU	7	610138216
21	25	FPGA 1, Connector 0, AI6-	↑	BLU/WHT	7	610138216
22	58	FPGA 1, Connector 0, AIGND6	30	SHIELD	7	610138216
23	23	FPGA 1, Connector 0, AI7-	30 T/P	VIO/WHT	8	610138216
24	57	FPGA 1, Connector 0, AI7+	↑	WHT/VIO	8	610138216
25	24	FPGA 1, Connector 0, AIGND7	30	SHIELD	8	610138216
26	55	FPGA 1, Connector 0, AO0	30 T/P	WHT/GRY	9	610138216
27	21	FPGA 1, Connector 0, AOGND0	↑	GRY/WHT	9	610138216
28	21	FPGA 1, Connector 0, AOGND0	26	AO GND	-	610138216
29	20	FPGA 1, Connector 0, AOGND1	30 T/P	BRN/RED	10	610138216
30	54	FPGA 1, Connector 0, AO1	↑	RED/BRN	10	610138216
31	19	FPGA 1, Connector 0, AOGND2	30 T/P	PNK/RED	11	610138216
32	53	FPGA 1, Connector 0, AO2	↑	RED/PNK	11	610138216
33	18	FPGA 1, Connector 0, AOGND3	30 T/P	ORG/RED	12	610138216
34	52	FPGA 1, Connector 0, AO3	↑	RED/ORG	12	610138216
35	17	FPGA 1, Connector 0, AOGND4	30 T/P	YEL/RED	13	610138216
36	51	FPGA 1, Connector 0, AO4	↑	RED/YEL	13	610138216
37	16	FPGA 1, Connector 0, AOGND5	30 T/P	GRN/RED	14	610138216
38	50	FPGA 1, Connector 0, AO5	↑	RED/GRN	14	610138216
39	15	FPGA 1, Connector 0, AOGND6	30 T/P	BLU/RED	15	610138216
40	49	FPGA 1, Connector 0, AO6	↑	RED/BLU	15	610138216
41	14	FPGA 1, Connector 0, AOGND7	30 T/P	VIO/RED	16	610138216
42	48	FPGA 1, Connector 0, AO7	↑	RED/VIO	16	610138216
43	2	FPGA 1, Connector 0, DGND	30 T/P	GRY/BRN	17	610138216
44	10	FPGA 1, Connector 0, DIO8	↑	BRN/GRY	17	610138216
45	2	FPGA 1, Connector 0, DGND	30 T/P	GRN/ORG	18	610138216
46	36	FPGA 1, Connector 0, DIO0	↑	ORG/GRN	18	610138216
47	3	FPGA 1, Connector 0, DGND	30 T/P	VIO/BRN	19	610138216
48	44	FPGA 1, Connector 0, DIO9	↑	BRN/VIO	19	610138216
49	3	FPGA 1, Connector 0, DGND	30 T/P	YEL/ORG	20	610138216
50	37	FPGA 1, Connector 0, DIO1	↑	ORG/YEL	20	610138216

Run #	From Location (Pin)	From Signal Desc	Wire AWG	Wire Color	Wire Group (PAIR)	To Location (Conn-Pin)
51	4	FPGA 1, Connector 0, DGND	30 T/P	BLU/BRN	21	610138216
52	11	FPGA 1, Connector 0, DIO10	↑	BRN/BLU	21	610138216
53	4	FPGA 1, Connector 0, DGND	30 T/P	GRY/PNK	22	610138216
54	38	FPGA 1, Connector 0, DIO2	↑	PNK/GRY	22	610138216
55	5	FPGA 1, Connector 0, DGND	30 T/P	GRN/BRN	23	610138216
56	45	FPGA 1, Connector 0, DIO11	↑	BRN/GRN	23	610138216
57	5	FPGA 1, Connector 0, DGND	30 T/P	VIO/PNK	24	610138216
58	39	FPGA 1, Connector 0, DIO3	↑	PNK/VIO	24	610138216
59	6	FPGA 1, Connector 0, DGND	30 T/P	YEL/BRN	25	610138216
60	12	FPGA 1, Connector 0, DIO12	↑	BRN/YEL	25	610138216
61	6	FPGA 1, Connector 0, DGND	30 T/P	BLU/PNK	26	610138216
62	40	FPGA 1, Connector 0, DIO4	↑	PNK/BLU	26	610138216
63	7	FPGA 1, Connector 0, DGND	30 T/P	ORG/BRN	27	610138216
64	46	FPGA 1, Connector 0, DIO13	↑	BRN/ORG	27	610138216
65	7	FPGA 1, Connector 0, DGND	30 T/P	GRN/PNK	28	610138216
66	41	FPGA 1, Connector 0, DIO5	↑	PNK/GRN	28	610138216
67	8	FPGA 1, Connector 0, DGND	30 T/P	PNK/BRN	29	610138216
68	13	FPGA 1, Connector 0, DIO14	↑	BRN/PNK	29	610138216
69	8	FPGA 1, Connector 0, DGND	30 T/P	YEL/PNK	30	610138216
70	42	FPGA 1, Connector 0, DIO6	↑	PNK/YEL	30	610138216
71	9	FPGA 1, Connector 0, DGND	30 T/P	GRY/RED	31	610138216
72	47	FPGA 1, Connector 0, DIO15	↑	RED/GRY	31	610138216
73	9	FPGA 1, Connector 0, DGND	30 T/P	ORG/PNK	32	610138216
74	43	FPGA 1, Connector 0, DIO7	↑	PNK/ORG	32	610138216
75	1	FPGA 1, Connector 0, +5v	26	GRN	-	610138216
76	22	FPGA 2, Connector 1, DGND	30	WHITE	-	610138216
77	35	FPGA 1, Connector 0, +5V	26	RED	-	610138216
78	56	FPGA 1, Connector 0, AISENSE	30	BLK	-	610138216
79	SHLD	OUTER SHIELD	24	BLK (6")	-	610138216